AW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/913,896	08/21/2001	Tsuyoshi Fujiwara	50140536X00	5967

7590 02/13/2004

Antonelli Terry Stout & Kraus
1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209

EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/913,896	FUJIWARA ET AL.
	Examiner	Art Unit
	Samuel A Gebremariam	2811

AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 20 November 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2,4-22,38,40-42 and 45-50 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2, 4-22, 38, 40-42 and 45-50 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9, 12-14, 16-19, 38 and 40-42, 45-48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. 6,287,951 in view of Matsubara US patent No. 6,274,417.

Regarding claim 1, Lucas teaches (fig. 9) a manufacturing process of a semiconductor device comprising: selectively forming a first insulating film (12) on a surface of a semiconductor substrate (10); forming a first conductor portion (14, 15) via a second insulating film (13) over the surface of the semiconductor substrate, forming a semiconductor region (16) in the semiconductor substrate, wherein the first insulating film and the first conductor portion do not exist; forming a third insulating film (22) to cover the first conductor portion, semiconductor layer and first insulating film; forming a fourth insulating film (24) over the third insulating film; forming a first opening in the fourth and third insulating films, forming a second conductor portion (82, 84, 86 and 88) in the first opening; and forming a fifth insulating film (26) over the fourth insulating film, where the fifth insulating film is formed using a silane, nitrogen and ammonia gas, while the third insulating film is formed using a silane and a nitrogen gas in an ammonia-free atmosphere (col. 4, lines 5-19).

Lucas does not explicitly teach the third and fifth insulating films are silicon nitride films formed by plasma CVD and the third insulating film is formed at a temperature higher than that of the fifth insulating film.

It is conventional and also taught by Matsubara (col. 1, line 62-64 and col. 2, line 30-34) forming silicon nitride using plasma CVD and thermal CVD. It is also known that CVD has a wide range of deposition temperature.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the third insulating layer in the process of Lucas at higher temperature in order to lower the water permeability of the silicon nitride.

Regarding claim 2, Lucas teaches substantially the entire claimed process of claim 1 above including the first (12) and fourth (24) insulating films are silicon oxide films, and the step for forming a first opening (61) (see fig. 6) comprises a step of etching the fourth insulating film under conditions permitting a larger etching amount of the fourth insulating film than that of the third insulating film and a step of etching the third insulating film under conditions permitting a larger etching amount of the third insulating film than that of the first insulating film.

Since the claimed process and materials are the same the process inherently permits a larger etching amount of the fourth insulating film than that of the third insulating film and a step of etching the third insulating film under conditions permitting a larger etching amount of the third insulating film than that of the first insulating film.

Regarding claim 4, Lucas teaches substantially the entire claimed process of claim 1 above including a step of forming a silicide laver over the surface of the semiconductor layer (col. 3, line 50-53).

Regarding claim 5, Lucas teaches substantially the entire claimed process of claim 1 above including the second conductor portion contains a first conductor layer (72) and a second conductor layer (74) and the first conductor layer is thinner than the second conductor layer and lies below the second conductor layer (fig. 7, col. 7, line 55-67, and col. 8, line 1-5).

Regarding claim 6, Lucas teaches (fig. 9) substantially the entire claimed process of claim 1 above including forming a third conductor portion (92) a step of connecting, in a second opening formed in the fifth insulating (26) film to expose a portion of the third conductor portion, the third conductor portion with an externally connecting conductor portion (96).

Regarding claim 7, Lucas teaches substantially the entire claimed process of claim 1 above including the first conductor portion (14 and 15) is formed of a silicon layer (col. 3, line 20-31).

Lucas does not explicitly teach the first conductor (14) contains boron.

It is conventional in the art to form gate structure of doped polysilicon material. Furthermore boron is well known dopant of polysilicon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the polysilicon gate with boron in the process of Lucas in order to increase the gate conductivity.

Regarding claim 8, Lucas teaches substantially the entire claimed process of claim 1 above including the first conductor portion (72 and 74) is formed of three conductor layers, that is, a first conductor layer made of silicon layer, a second conductor layer of metal nitride (tantalum nitride) and a third conductor layer made of a refractory metal (col. 7, line 55-67).

Regarding claims 9 and 47, Lucas teaches substantially the entire claimed process of claims 1 and 2 above except explicitly teaching that the third and fifth insulating films are silicon nitride films formed by plasma CVD and the third insulating film has hydrogen content smaller than that of the fifth insulating film.

Matsubara has established that hydrogen has a detrimental effect to a MOSFET structure because water diffuses into the gate oxide film to increase Si-H combination (col. 1, line 26-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the third insulating film with less hydrogen content in the process of Lucas in order to reduce the silicon-hydrogen combination, which has a detrimental effect to the gate structure.

Regarding claim 12, Lucas teaches substantially the entire claimed process of claim 1 above except explicitly teaching that the second insulating film (22) (same as the third insulating film of claim 1) is a silicon nitride film formed by plasma CVD at 400°C or greater.

Furthermore Lucas has established that silicon nitride can be formed using reaction gas having silane and nitrogen gas in an ammonia-free atmosphere (col. 4, lines 5-19).

Parameters such as deposition temperature and annealing temperature in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon nitride of Lucas process at the temperature as claimed in order to form a device that less prone to failure.

Regarding claims 13 and 14, Lucas teaches substantially the entire claimed process of claims 1 and 3 above including the second insulating film is formed using a reaction gas having monosilane and nitrogen (the 2nd and 3rd insulating films are the same as the 3rd and 4th of insulating films of claim 2).

Regarding claims 16 and 17, Lucas teaches substantially the entire claimed process of claims 1 and 5 above including the first conductor layer is a titanium nitride layer (72), while the second conductor layer is a tungsten layer (74) (col. 7, line 55-67).

Regarding claims 18 and 19, Lucas teaches (fig. 9) a manufacturing process of a semiconductor device comprising: selectively forming an element isolation regions (12) on a surface of a semiconductor substrate (10); forming a gate electrode (14, 15) via a second insulating film (13) over the surface of the semiconductor substrate, forming a source and drain region (16) in the semiconductor substrate by introducing impurities, forming a first insulating film (22) to cover the gate electrode, source/drain region and

element isolation regions; forming a second insulating film (24) over the first insulating film; wherein the first insulating film is formed using a silane, nitrogen and ammonia gas, while the third insulating film is formed using a silane and a nitrogen gas in an ammonia-free atmosphere (col. 4, lines 5-19).

Lucas does not explicitly teach the first insulating film is formed by plasma CVD. It is conventional and also taught by Matsubara (col. 1, line 62-64 and col. 2, line 30-34) forming silicon nitride using plasma CVD and thermal CVD.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first insulating layer in the process of Lucas using plasma CVD as taught by Matsubara in order to have better coverage as opposed to line sight deposition process.

Regarding claim 38, Lucas teaches substantially the entire claimed process of claims 1 and 12 above including forming a first conductor portion (14, 1501-1503) made of a silicon material, wherein a high refractory silicide layer is formed on the surface of the first conductor portion (col. 3, line 20-31).

Regarding claims 40-42 and 50, Lucas teaches substantially the entire claimed process of claims 1 and 12 above including forming a first (22) and a second (26) silicon nitride films. Lucas further teaches that (col. 4, line 5-19) that silicon nitride can be formed using either silane with nitrogen gas or silane with ammonia and nitrogen gas.

Matsubara further teaches that silicon nitride can be formed using plasma CVD.

Lucas does not explicitly teach the first silicon nitride film is formed by plasma CVD using a raw material gas having silane and nitrogen, and the second silicon nitride

film is formed by plasma CVD using a raw material gas having silane, ammonia and nitrogen.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first silicon nitride film using a raw material gas having silane and nitrogen as claimed in the process of Lucas in order to reduce the silicon-hydrogen combination that may arise from the ammonia source, which has a detrimental effect to the gate structure and further using raw material gas having silane, nitrogen and ammonia for the second silicon nitride in order to form a barrier layer.

The limitation of forming first silicon nitride film for self alignment and forming second silicon nitride film for passivation is not given patentable weight since a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 45 and 46 Lucas teaches substantially the entire claimed process of claims 1 and 9 above including the second insulating film is formed using a reaction gas having monosilane and nitrogen.

Claims 15 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas and Matsubara in view of Hashimoto US patent No. 5,717,254.

Regarding claims 15 and 48, Lucas teaches (col. 3, line 50-53) substantially the entire claimed process of claims 1 and 2 above except stating the details of the silicide-forming step.

Hashimoto teaches (fig. 3A, col. 7, line 51-62) depositing a refractory metal film over the semiconductor layer and first insulating film; heat treating the semiconductor substrate, thereby forming a silicide layer over a surface of the semiconductor layer; and removing the refractory metal film over the first insulating film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process steps of silicidation process taught by Hashimoto in the process of Lucas in order to reduce contact resistance between interconnect structure and the semiconductor layer during further metallization process.

Claims 10, 11, 20-22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas in view of Matsubara.

Regarding claims 10 and 11, Lucas teaches a manufacturing process of a semiconductor device according to the present invention, comprises: forming a first insulating film (22) on a surface of a semiconductor substrate (1); forming a second insulating film (24) over the first insulating film; forming an opening in the second and first insulating films; forming a conductor layer (82, 84, 86 88) in the opening; and forming a third insulating film (26) over the conductor layer, wherein the first insulating film and the third insulating film are silicon nitride films formed by plasma CVD and the first insulating film is formed at a temperature higher than that of the third insulating film and the first insulating film has a hydrogen content smaller than that of the third

insulating film (see also rejection for claims 1 and 9) where the fifth insulating film is formed using a silane, nitrogen and ammonia gas, while the third insulating film is formed using a silane and a nitrogen gas in an ammonia-free atmosphere (col. 4, lines 5-19).

Regarding claims 20, 21 and 49, Lucas teaches substantially the entire claimed process of claims 10, 13 and 18 above including the second insulating film (24) is a silicon oxide film.

Regarding claim 22, Lucas teaches (fig. 7) substantially the entire claimed process of claim 20 above including the conductor forming step comprises forming a first conductor layer as a lower layer (72) and a second conductor layer as an upper layer (74), the second conductor layer is made of copper, and the first conductor layer serves to prevent diffusion of copper (col. 7, line 55-67).

Response to Arguments

3. Applicant's arguments filed 11/20/03 have been fully considered but they are not persuasive. Applicant argues that the combined reference of Lucas and Matsubara teach the limitation of forming a silicon nitride film using gases that include silane, nitrogen but not ammonia using the well established process CVD process. As stated clearly in col. 4, lines 5-19, Lucas teaches the range of possibilities on how to go about forming silicon nitride layer. Lucas states that the nitrogen source gas can just be N2 for forming silicon nitride and silicon source would be silane. Therefore Lucas explicitly teaches that silicon nitride can be formed using gas precursors that are free of ammonia. Furthermore Matsubara (col. 1, line 62-64 and col. 2, line 30-34) teaches

forming silicon nitride using plasma CVD method. Therefore a person of ordinary skill in the would be motivated to combine the process steps of Lucas and Matsubara in order form a semiconductor device free of problems caused by hydrogen from the ammonia gas.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571)) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 9, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800